IOSR Journal of Electrical and Electronics Engineering (IOSR-JEEE)
e-ISSN: 2278-1676,p-ISSN: 2320-3331
PP 19-27
www.iosrjournals.org

A Step-Up Switched-Capacitor Multilevel Inverter with Self Voltage Balancing

Vengatesan.G[1], Sathish Kumar.G.K[2],
PG scholar[1], Asst Professor [2],
Arunai College of Engineering, Thiruvannamalai.

Abstract: *This paper addresses the control requirements of hybrid wind farms comprising a relatively the Permanent Magnet Synchronous Generator (PMSG), capable of compensating the reactive power demanded by the IMs during faulty conditions as well as attenuating the active power variations due to wind velocity. Based on the superposition theorem and the feedback linearization technique, a controller is designed to independently regulate the positive and negative sequence currents of the PMSG voltage source converters (VSC), overcoming several drawbacks of existing approaches in the presence of unbalanced voltages. In the proposed scheme, the grid-side VSC currents are controlled in order to improve the ride-through capability of IM so that the whole wind farm can fulfil demand. As the IM based wind farms with PMSG accomplishes several relevant goals delivering the reactive power consumption of the IM increasing the rated active power of the installation, and smoothing mechanical power oscillations. Then the objective of this system is to propose a new inverter topology for a multilevel voltage output. This topology is designed based on a switched capacitor (SC) technique, and the number of output levels is determined by the number of SC cells. Only one dc voltage source is needed, and the problem of capacitor voltage balancing is avoided as well. This structure is not only very simple and easy to be extended to a higher level, but also its gate driver circuits are simplified because the number of active switches is reduced. The operational principle of this inverter and the targeted modulation strategies are presented, and power losses are investigated. Finally, the performance of the proposed multilevel inverter is evaluated with the experimental results of an 11-level prototype inverter.*

Keywords: *Static Synchronous Compensator (STATCOM), Permanent Magnet Synchronous Generator (PMSG), Fundamental Frequency Modulation (FFM*

I. Introduction

In co-operation of electric utilities and end users of electric power are increasing worried about the quality of power. Power quality can be defined as "any power problem maintained in voltage, current and frequency those results in failure or mal operation of the customer equipment" [1]. Addition of the wind power into an electric grid affects the power quality. The assembly of devices used for improvement of power quality problems is known by the name of Custom Power Devices (CPD). The family of compensating devices mainly has the following members: Static Synchronous Compensator (STATCOM), Dynamic Voltage Restorer (DVR) and Unified Power Quality Conditioner (UPQC). The occupation analyses the presentation of Static Compensator (STATCOM) with a battery energy storage system (BESS) connected at the point of common coupling of wind energy generating system and the obtainable power system to alleviate the power quality issues throughout the normal operation, wind turbine produces an incessant variable output power. The most important power quality issues are voltage sag, swell, flickers, and harmonics one of the straightforward methods of running a wind generating system is to use the induction generator connected directly to the grid. The induction generator has inherent advantages of cost efficiency and heftiness. But, induction generators require reactive power designed for magnetization. [2]

In order to investigate the feasibility of improving the ride-through capability and the active power smoothness of WECS by incorporating a PMSG-WECS, the control strategy is focused on the grid-side VSC, which is exposed to both balanced and unbalanced electric network faults. Most of the VSC controllers under unbalanced conditions can be classified in two categories. The first one, based on a dual sequence control (DSC) scheme independently controls the positive and negative sequences using two reference frames rotating at synchronous speed, but in opposite directions. The second category of methods uses Proportional plus Resonant (PR) controllers which allow tracking, without steady-state error, constant and sinusoidal current references arising in synchronous frames under unbalanced conditions. In several PMSG-WECS control approaches the unbalanced conditions in the electric network are not taken into account. In order to improve the performance of PMSG-WECS applications the same strategies are presented, considering that the grid-side VSC is connected to an unbalanced voltage [3]. However, these works deal only with the dc-link voltage control and an arbitrary

injection of power to the grid. In this paper, a thorough analysis is presented related to how a WECS can meet the grid code requirements through the inclusion of a PMSG-WECS. The active and reactive power references to be injected by the grid-side VSC are designed so that the whole wind farm, composed of both sorts of machines, can meet the current grid codes. Besides, the grid-side VSC control for tracking these power references is tailored for overcoming balanced and unbalanced faults which can arise in the electric network. To this end, the DSC scheme is chosen in the grid-side VSC controller design. The inclusion of the PMSG, along with its back-to-back converter, can enlarge the active power capacity of existing farms while providing the reactive power support during network faults and smoothing the active power output when wind velocity occurs. [4] In recent years, numerous new multilevel inverter topologies that cannot be attributed to the traditional three classifications aforementioned have been reported. Specifically, multiple sub multi-level converter units and full bridge converters are employed in the new multilevel inverter topology. In a simple topology is proposed, but multiple separated dc voltage sources are still required. The coupled-inductor technique used in multilevel inverters was introduced. The structures are simplified, but it is difficult to expand this technique to higher level applications. In novel topologies based on switched capacitor (SC) and boost techniques were presented, but their numbers of output voltage levels are limited at 13, 7, and 5, respectively. In contrast, the multilevel topology introduced in can be extended to higher levels. However, the use of a large number of active switches increases the cost and component counts in terms of gate driver circuits and the overall system. Based on the SC technique that has been applied in many applications, a novel multilevel inverter topology connecting a multilevel dc–dc converter and a full bridge is presented in this paper. With the proposed topology, only one dc voltage source is required, and many other problems, such as voltage balancing, numerous active switches, and complex gate driver circuits, are avoided. The dc–dc conversion section is the key point of the whole topology, which is designed by connecting multiple SC cells. Each SC cell consists of a capacitor, an active switch, and two diodes. Consequently, the output voltage levels of the proposed inverter could be flexibly varied by employing different numbers of SC cells.

II. Proposed System

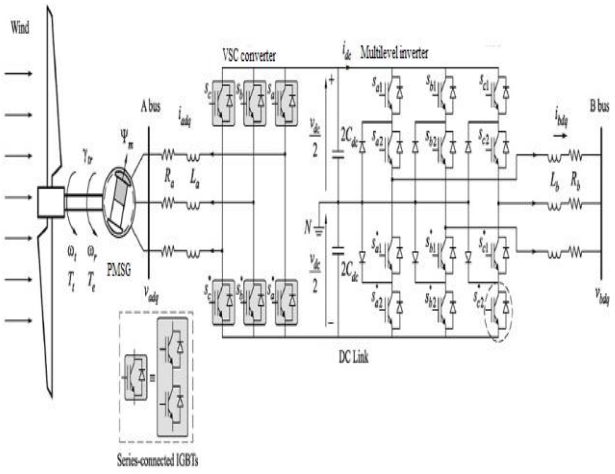

Fig 1: Proposed system block diagram

2.1 Wind Energy Conversion

Wind turbines capture power from the wind by means of aerodynamically designed blades and convert it to rotating mechanical power. The number of blades is three in a modern wind turbine. For multi-MW wind turbines the rotational speed is typically 10-15 rpm. The most weight efficient way to convert the low-speed, high-torque power to electrical power is to use a gear-box and a standard generator including a power electronic interface. The gear-box is optional as multi-pole generator systems are also possible solutions. Between the grid and the generator a power converter can be inserted. The electrical output can either be AC or DC.
The available power of wind energy system is presented as

$$P_{Available} = \frac{1}{2} \cdot \rho \cdot A \cdot V^3 \quad \text{.....(1)}$$

Where ρ= air density (kg/m3) , A = area swept out by turbine blade (m), V= wind speed (m/s).It is not possible to extract all kinetic energy of wind.

$$P_m = \frac{1}{2} \cdot C_p \cdot \rho \cdot A \cdot V^3$$ ……..(2)

Thus extracts a fraction of the power called power coefficient „Cp" of the wind turbine, and is given by

$$C_p = \frac{P_m}{P_{Available}}$$ ……(3)

$$\lambda = \frac{\omega_r \cdot R}{V}$$ ……..(4)

The mechanical power produced by wind turbine is given by
Where, R = Radius of the blade (m).

2.2 Power Converter Topology

Basically two power converter topologies with full controllability of the generated power are currently used in the commercial wind turbine systems. These power converters are related to the partial-rating power converter wind turbine and the full-rating one. However, other topologies have been proposed in the last years.

A. Bi-directional back-to-back two-level power converter

The back-to-back Pulse Width Modulation-Voltage Source Converter (PWM-VSC) is a bi-directional power converter consisting of two conventional PWM-VSC. The PWM-VSC is the most frequently used three-phase frequency converter. As a consequence of this, the knowledge available in the field is extensive and very well established. Furthermore, many manufacturers produce components especially designed for use in this type of converter (e.g., a transistor-pack comprising six bridge coupled transistors and anti-paralleled diodes). Therefore, the component costs can be low compared to converters requiring components designed for a niche production. A technical advantage of the PWM-VSC is the capacitor decoupling between the grid inverter and the generator inverter. Besides affording some protection, this decoupling offers separate control of side, independently. The inclusion of a boost inductance in the DC-link circuit increases the component count, but a positive effect is that the boost inductance reduces the demands on the performance of the grid side harmonic filter, and offers some protection of the converter against abnormal conditions on the grid. However, some disadvantages of the back-to-back PWMVSC are reported in literature e.g. [1] and [3]. In several papers concerning adjustable speed drives, the presence of the DC-link capacitor is mentioned as a drawback, since: it is bulky and heavy; - it increases the costs and maybe of most importance; - it reduces the overall lifetime of the system. Another important drawback of the back-to-back PWMVSC is the switching losses. Every commutation in both the grid inverter and the generator inverter between the upper and lower DC-link branch is associated with a hard switching and a natural commutation. Since the back-to-back PWM-VSC consists of two inverters, the switching losses might be even more pronounced. The high switching speed to the grid may also require extra EMI-filters.

B. Multilevel power converter

In Currently, there is an increasing interest in multilevel power converters especially for medium to high-power, high-voltage wind turbine applications [7]. Since the development of the neutral-point clamped three level converter, several alternative multilevel converter topologies have been reported in the literature. The general idea behind the multilevel converter technology is to create a sinusoidal voltage from several levels of voltages, typically obtained from capacitor voltage sources. The different proposed multilevel converter topologies can be classified in the following five categories [6] multilevel configurations with diode clamps, multilevel configurations with bi-directional switch interconnection, multilevel configurations with flying capacitors, multilevel configurations with multiple three-phase inverters and multilevel configurations with cascaded single phase H-bridge inverters.

Initially, the main purpose of the multilevel converter was to achieve a higher voltage capability of the converters. As the ratings of the components increases and the switching- and conducting properties improve, the secondary effects of applying multilevel converters become more and more advantageous. The reduced content of harmonics in the input and output voltage as well as a reduced EMI is reported [1]. The switching losses of the multilevel converter are another feature, which is often accentuated in literature. In it is stated, that for the same harmonic performance the switching frequency can be reduced to 25% of the switching frequency

of a two-level converter. Even though the conduction losses are higher for the multilevel converter, the overall efficiency for the diode clamped multilevel converter is higher than the efficiency for a comparable two-level converter [1]. However, this depends on the ratio between the switching losses and the conduction losses.

C. Dc link

The most commonly reported disadvantage of the three level converters with split DC-link is the voltage imbalance between the upper and the lower DC-link capacitor. Nevertheless, for a three-level converter this problem is not very serious, and the problem in the three-level converter is mainly caused by differences in the real capacitance of each capacitor, inaccuracies in the dead time implementation or an unbalanced load. By a proper modulation control of the switches, the imbalance problem can be solved. In the voltage balancing problem is solved by hardware, while proposed solutions based on modulation control. The three-level diode clamped multilevel converter and the three-level flying capacitor multilevel converter exhibits an unequal current stress on the semiconductors. It appears that the upper and lower switches in an inverter branch might be de-rated compared to the switches in the middle. For an appropriate design of the converter, different devices are required. The unequal current stress and the unequal voltage stress might constitute a design problem for the multilevel converter with bidirectional switch interconnection presented. It is evident for all presented topologies in that the number of semiconductors in the conducting path is higher than for e.g. a two-level converter. Thus, the conduction losses of the converter might increase. On the other hand, each of the semiconductors need only to block half the total DC-link voltage and for lower voltage ratings, the on-state losses per switch decreases, which to a certain extent might justify the higher number of semiconductors in the conducting path.

III. Proposed Multilevel Iverter

The proposed multilevel inverter is cascaded by a dc–dc multilevel converter and a full bridge, as shown in Fig. 1. For its dc–dc converter section that consists of the number of n SC cells, it is capable of providing the number of n + 1 voltage levels according to different switching states. With the operation of the H-bridge, a total of 2n + 3 voltage levels can be produced, i.e., 0,±Vin,±2Vin, . . . ,±(n + 1)Vin. Without loss of generality, the following assumptions have been made for analysis.

- The values of all SCs Ci are large enough, and the voltage ripples across them are negligible.
- All the switching devices are ideal, i.e., no ON-state voltage drop and on-resistance.
- Input power source Vin is ideal, i.e., it is constant and there is no series impedance.

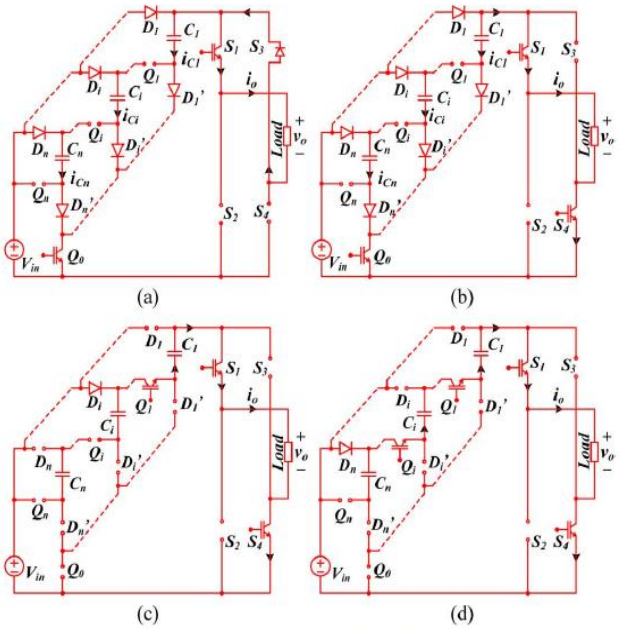

Fig 2: (a) Zero-Level Output (b) First Level of Output(±Vin) (c) Second Level of Output(±i × Vin) (d)Final Level of Output (±(n + 1)Vin)

A. Zero-Level Output

When switch Q0 is turned ON while Qi(i = 1, 2, . . . , n) is OFF, all SCs Ci are charged by input power source Vin through diodes Di and D_ i, as shown in Fig. 2(a). For the H-bridge, only switch S1 is turned ON,

whereas the others are OFF. There is no voltage developed for the load. The output voltage is therefore equal to zero. Output current iO can be freewheeling through S1 and the bypass diode of S3 when the load is not pure resistance. There is also another zero level that can be produced by turning ON S2 while the other switches are OFF.

B. First Level of Output (±Vin)

For the dc–dc conversion section, its operating state is the same as that for the zero-level state aforementioned, i.e., Q0 maintains the ON-state while the other switches are OFF. The voltages across capacitors Ci are eventually equal to input voltage Vin, i.e., VCi = Vin (i = 1, 2 . . . n). For the H-bridge, switches S1 and S4 are turned ON simultaneously, whereas S2 and S3 maintain the OFF-state. Voltage Vin is developed by the input power directly to the load, as shown in Fig. 2(b). Similarly, the level of −Vin can be developed by turning ON switches S2 and S3, whereas S1 and S4 are OFF.

C. Second Level of Output (±i × Vin)

When switch Q0 is turned OFF, voltage level i × Vin can be developed in the dc–dc conversion section by turning ON switches Q1–Qi−1 (i = 2, 3 . . . n), whereas Qi–Qn are OFF. In this case, capacitors C1–Ci−1 are connected in series with input source Vin, and the total voltage level, i.e., Vin + VC1 + · · · + VCi−1, is produced. Based on the aforementioned assumption, the voltages across all capacitors are the same as input voltage Vin. This total voltage level is therefore equal to i × Vin. With the operation of the full bridge, this voltage level can be developed to the load by turning ON S1 and S4, whereas S2 and S3 are OFF, as shown in Fig. 2(b). The level of −i × Vin can be also provided to the load by controlling the full bridge in a reverse manner. In particular, when i = n, the output level is equal to ±nVin, as shown in Fig. 2(c).

DFinal Level of Output (±(n + 1)Vin)

For the dc–dc section, the highest voltage level (n + 1)Vin can be obtained by connecting all capacitors Ci in series with input Vin when switches Q1–Qn are all turned ON, whereas Q0 maintains the OFF-state, as shown in Fig. 2(d). Based on the aforementioned analysis, the positive and negative levels, i.e., ±(n + 1)Vin, can be generated by turning ON S1 and S4 or S2 and S3.

3.2 FFM for Proposed Inverter Switching Technique

For the FFM fundamental frequency modulation (FFM). methods, a staircase voltage waveform is generated by connecting different numbers of capacitor sources to the output terminal and with only one or two commutations of active switches during one cycle of the fundamental output

voltage. A representative of this family is the selective harmonic elimination (SHE) method [6]. It was also introduced to modulate the proposed inverter to output a staircase voltage. For a staircase waveform with z steps, its Fourier transform can be expressed as

$$v_1(\omega t) = \frac{4V_{\text{in}}}{\pi}\left[\cos(\theta_1) + \cos(\theta_2) + \cdots + \cos(\theta_Z)\right]\sin(\omega t) \quad \ldots.(5)$$

where k = 1, 3, 5, 7, . . . are odd numbers. θ1, θ2 to θZ are the conducting angles for each step of the staircase waveform.

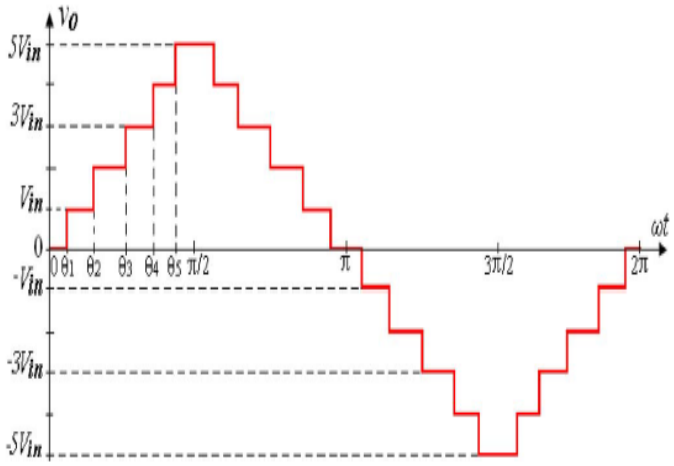

Fig 3: Staircase Waveform

IV. Simulation Results

4.1Multilevel inverter based PMSG wind farm with self load balancing

This Simulink diagram states that PMSG wind generator 6KW, 400V connected to the grid with the STATCOM and according to the wind velocity 10m/sec its influences in the system under steady state on the grid. The following figure shows the voltage waveform of grid which is subjected to grid connected PMSG wind generating system with the use of 11lelvel multilevel inverter based on STATCOM. The figure represents the rectifier unit having of 2mH, 200microF power waveform of grid connected PMSG which is operated under asymmetrical grid.

A.Pmsg – Permanent Magnet Synchronous Generator

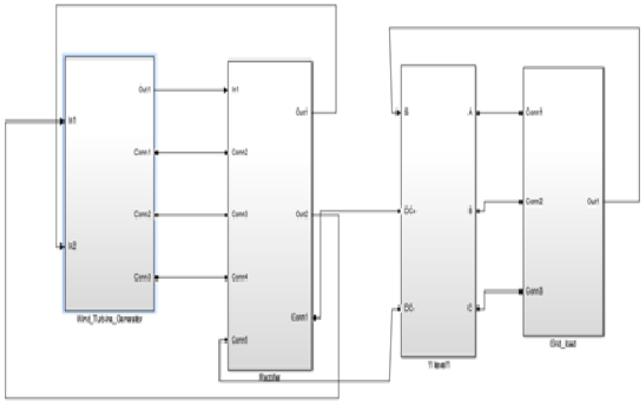

FIG 4: Block Diagram of PMSG Generation Model

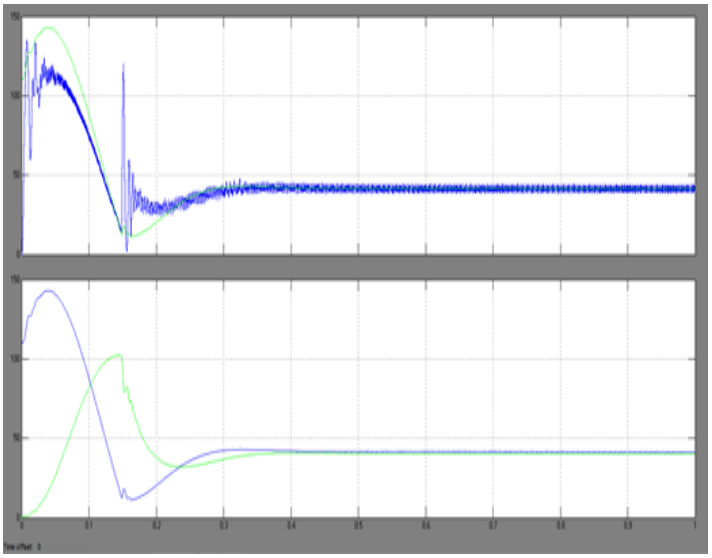

FIG 5: Output Waveform of Wind Turbine Generator Terminal

B.PMSG - Rectifier:

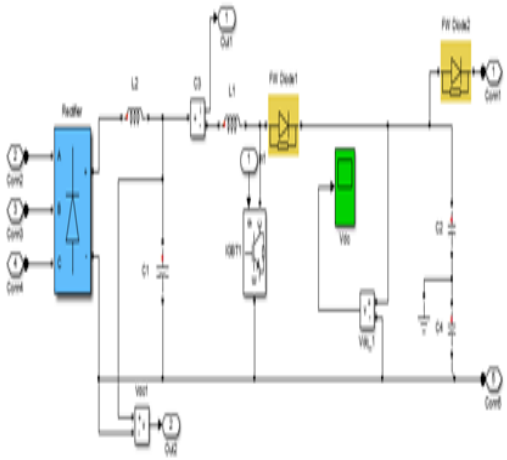

FIG 6: Block Diagram of PMSG Rectifier

C. Multi – Level Converter:

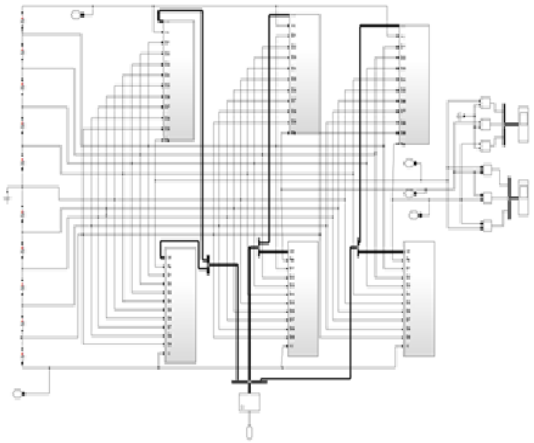

FIG 7: Block Diagram Of 11 Level Inverter

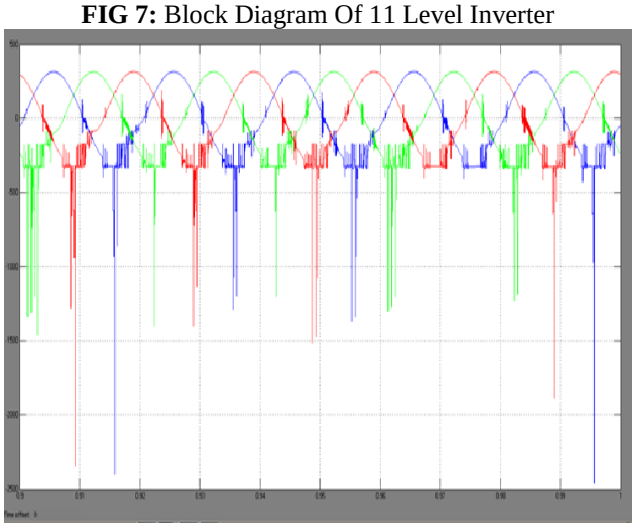

FIG 8: Output Waveform of 11 Level Converter in PMSG – With Ground

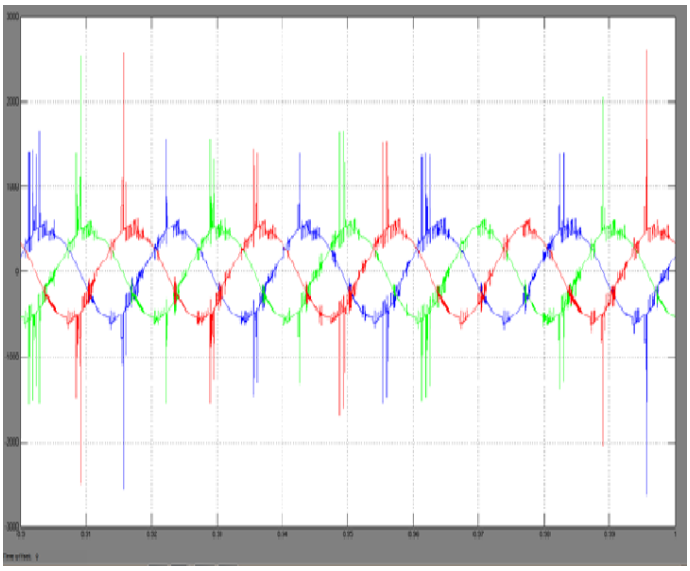

FIG 9: Output Waveform of 11 Level Converter in PMSG – Without Ground

D. Pmsg – Grid Load:

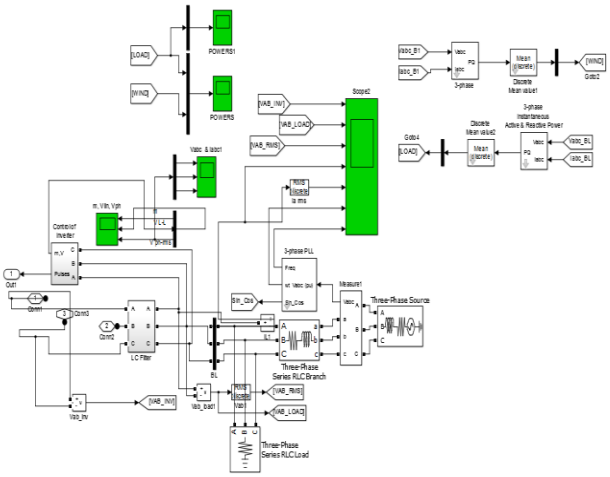

FIG 9: Block Diagram of PMSG Grid Load

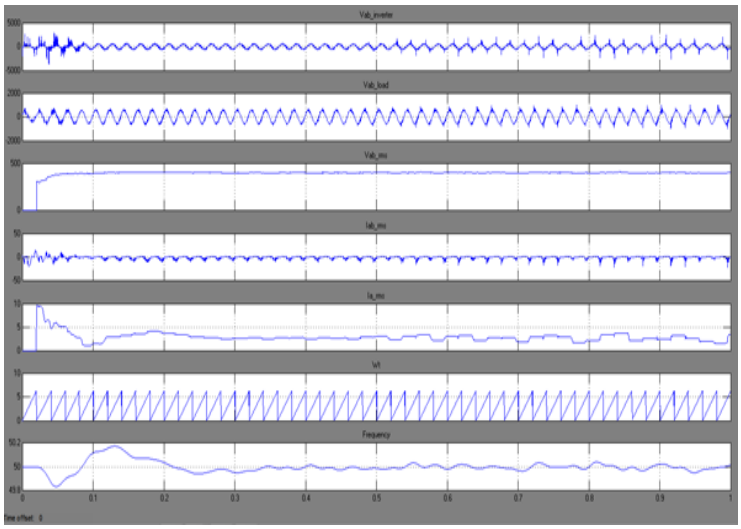

FIG 10: Grid Load Waveform of PMSG

V. Conclusion

This paper proposes the control strategies of the back to- back PWM converters in PMSG wind power system, for the grid voltage faults and for the MPPT. At the grid fault, a method is based on the DC-link voltage control at the machine-side converter, using feedback linearization technique. The MPPT strategy, where a proportional controller is added to the torque controller to improve the dynamic performance of the MPPT control, is developed to control the grid power at the grid-side converter. The validity of the simulation has been verified results for PMSG wind power system. The output voltage level could be varied flexibly. It has been analysed that the proposed inverter provides 2n + 3 levels on the output voltage, using only n capacitors and n + 5 active switches. Finally, the operation and performance of the proposed inverter are verified with experiments on an 11-level inverter prototype. Although good performance could be obtained in both the high switching frequency and fundamental switching frequency modes, it can be seen that the presented inverter is more suitable for the latter modulation method by comparing the experimental results. Experimental waveforms also indicate that the load capacity of the inverter declines with the decrease in the output frequency. Therefore, the proposed inverter is more suitable for high-frequency applications.

References

[1]. E.Ribeiro, A. J. M. Cardoso, and C.Boccaletti, "Fault-tolerant strategy for a photovoltaic DC–DC converter," IEEE Trans. Power Electron., vol. 28, no. 6, pp. 3008–3018, Jun. 2013.

[2]. H.Wu and X. He, "Single phase three-level power factor correction circuit with passive lossless snubber," IEEE Trans. Power Electron., vol. 17, no. 6, pp. 946–953, Nov. 2002.

[3]. J. M. Kwon, B. H. Kwon, and K. H. Nam, "Three-Phase photovoltaic system with three-level boosting MPPT control," IEEE Trans. Power Electron., vol. 23, pp. 2319–2327, Sep. 2008.

[4]. W. Li and X. He, "Review of non-isolated high-step-up DC/DC converters in photovoltaic grid-connected applications," IEEE Trans. Ind. Electron., vol. 58, no. 4, pp. 1239–1250, Apr. 2011.

[5]. M. H. Todorovic, L. Palma, and P. N. Enjeti, "Design of a wide input range DC–DC converter with a robust power control scheme suitable for fuel cell power conversion," IEEE Trans. Ind. Electron., vol. 55, no. 3, pp. 1247–1255, Mar. 2008.

[6]. M. T. Zhang, Y. Jiang, F. C. Lee, and M. M. Jovanovic, "Single-phase three-level boost power factor correction converter," in Proc. IEEE APEC, 1995, pp. 434–439.

[7]. A. Shahin, M. Hinaje, J. P. Martin, S. Pierfederici, S. Rael, and B. Davat, "High voltage ratio DC–DC converter for fuel-cell applications," IEEE Trans. Ind. Electron., vol. 57, pp. 3944–3955, Dec. 2010.

[8]. V.Yaramasu and B.Wu, "Three-Level boost converter based medium voltage megawatt PMSG wind energy conversion systems," in Proc. Energy Converters. Congr. Expo. (ECCE), 2011, pp. 561–567.

[9]. CHINCHILLA, M., S. ARNALTES and J.C. BURGOS. Control of permanent-magnet generators applied to variable-speed wind energy systems connected to the grid. IEEE Transactions on Energy Conversion. 2006, vol. 21, iss. 1, pp. 130–135. ISSN 0885-8969. DOI: 10.1109/TEC.2005.853735.

[10]. POLINDER, H., F. F. A VAN DER PIJL and P. TAVNER. Comparison of direct-drive and geared generator concepts for wind turbines. IEEE Transactions on Energy Conversion. 2006, vol. 21, iss. 3, pp. 725–733. ISSN 0885-8969. DOI: 10.1109/TEC.2006.875476.